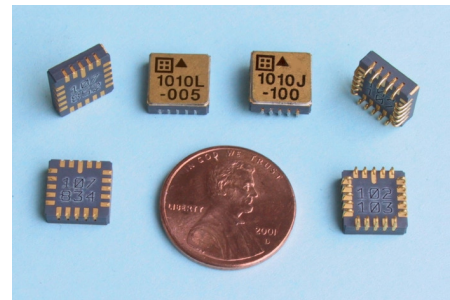




- Capacitive Micromachined
- Nitrogen Damped
- Hermetically Sealed
- Digital Pulse Density Output
- Fully Calibrated
- Responds to DC & AC Acceleration
- -55 to +125 °C Operation
- +5 VDC, 2 mA Power (typical)
- Non-Standard g Ranges Available
- Integrated Sensor & Amplifier
- LCC or J-Lead Surface Mount Package
- Serialized for Traceability
- TTL/CMOS Compatible
- No External Reference Voltage
- Easy Interface to Microprocessors
- Good EMI Resistance
- RoHS Compliant



Available G-Ranges

| Full Scale Acceleration | 20 pin LCC | 20 pin JLead |
|-------------------------|------------|--------------|
| ± 2 g | 1010L-002 | 1010J-002 |
| ± 5 g | 1010L-005 | 1010J-005 |
| ± 10 g | 1010L-010 | 1010J-010 |
| ± 25 g | 1010L-025 | 1010J-025 |
| ± 50 g | 1010L-050 | 1010J-050 |
| ±100 g | 1010L-100 | 1010J-100 |
| ±200 g * | 1010L-200 | 1010J-200 |

* Recommended for Down Hole Drilling

DESCRIPTION

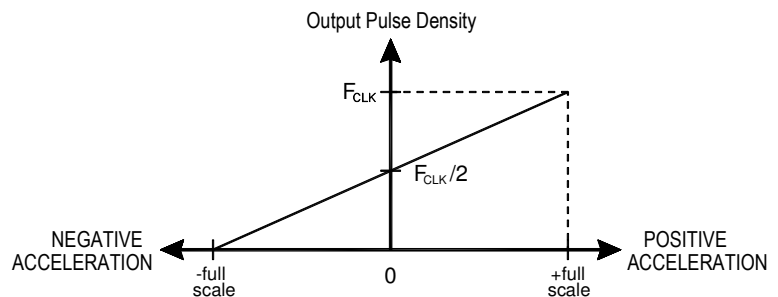
The Model 1010 is a low-cost, integrated accelerometer for use in zero to medium frequency instrumentation applications. Each miniature, hermetically sealed package combines a micro-machined capacitive sense element and a custom integrated circuit that includes a sense amplifier and sigma-delta A/D converter. It is relatively insensitive to temperature changes and gradients. Each device is marked with a serial number on its bottom surface for traceability. An optional calibration test sheet (1010-TST) is also available which lists the measured bias, scale factor, linearity, operating current and frequency response.

OPERATION

The Model 1010 produces a digital pulse train in which the density of pulses (number of pulses per second) is proportional to applied acceleration. It requires a single +5 volt power supply and a TTL/CMOS level clock of 100kHz-1MHz. The output is ratiometric to the clock frequency and independent of the power supply voltage. Two forms of digital signals are provided for direct interfacing to a microprocessor or counter. The sensitive axis is perpendicular to the bottom of the package, with positive acceleration defined as a force pushing on the bottom of the package. External digital line drivers can be used to drive long cables or when used in an electrically noisy environment.

APPLICATIONS

- Automotive
 - Air Bags
 - Active Suspension
 - Adaptive Brakes
 - Security Systems
- Shipping Recorders
- Appliances
- Vibration Monitoring
- Vibration Analysis
- Machine Control
- Modal Analysis
- Robotics
- Crash Testing
- Instrumentation



SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE



PERFORMANCE

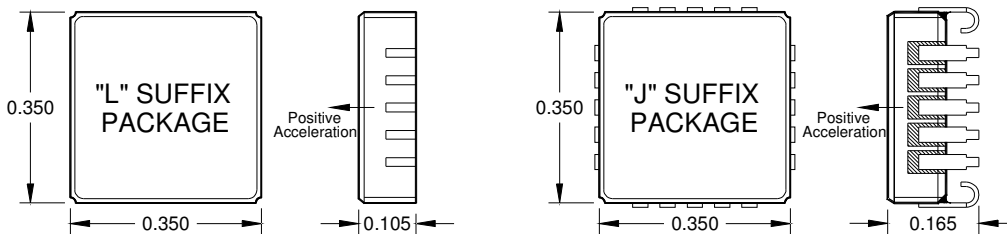
By Model: V_{DD}=V_R=5.0 VDC, F_{CLK}=250 kHz, T_C=25°C.

Table with 5 columns: Model Number, Input Range, Frequency Response (Nominal, 3 dB), Sensitivity (F_{CLK}=250kHz), Max. Mechanical Shock (0.1 ms). Rows include models 1010-002 through 1010-200.

All Models: Unless otherwise specified V_{DD}=V_R=5.0 VDC, F_{CLK}=250 kHz, T_C=25°C.

Table with 6 columns: PARAMETER, MIN, TYP, MAX, UNITS. Rows include Cross Axis Sensitivity, Bias Calibration Error, Bias Temperature Shift, Scale Factor Calibration Error, Scale Factor Temperature Shift, Non-Linearity, Power Supply Rejection Ratio, Operating Voltage, Operating Current, Clock Input Voltage Range, and Mass.

Note 1: Tighter tolerances available on special order. Note 2: 100g and greater versions are tested from -65 to +65g.

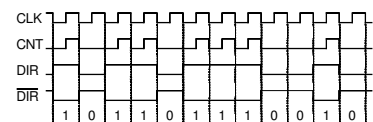


SIGNAL DESCRIPTIONS

VDD and GND (power): Pin 14 (VDD) & pin 19 (GND). Additionally tie pins 3 & 11 to VDD & pins 2, 5, 6 & 18 to GND.

CLK (input): Pin 8. Reference clock input. This hysteresis threshold input must be driven by a 50% duty cycle square wave signal. Factory Calibration is performed at 250 kHz, which is the recommended clock frequency for best results.

CNT (output): Pin 10. Count output. A return-to-zero type digital pulse stream whose pulse width is equal to the input CLK logic high time. The CNT pulse rate increases with positive acceleration.



DIR and DIR (output): Pins 12 & 16 respectively. Direction output. This output is updated at the fall of each clock cycle. It is high during clock cycles when a high going CNT pulse is present and low during cycles when no CNT pulse is present.

SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE



return-to-zero signal meant to control the count direction (i.e. up or down) of a counter. DIR can be low pass filtered to produce an analog measure of the acceleration. \overline{DIR} is the complement of DIR and is provided for use in driving differential transmission lines.

DV (input): Pin 4. Deflection Voltage. Normally left open. A test input that applies an electrostatic force to the sense element, simulating a positive acceleration. The nominal voltage at this pin is $\frac{1}{2}V_{DD}$. DV voltages higher than required to bring the output to positive full scale may cause device damage.

VR (input): Pin 3. Voltage Reference. Tie directly to V_{DD} (+5V). A 0.1 μ F bypass capacitor is recommended at this pin.

CLK/2 (output): Pin 15. Clock divided by 2. A buffered clock output whose frequency equals CLK divided by 2.

ABSOLUTE MAXIMUM RATINGS *

| | |
|--|------------------------|
| Case Operating Temperature | -55 to +125°C |
| Storage Temperature | -55 to +125°C |
| Acceleration Over-range | 2000g for 0.1 ms |
| Voltage on V_{DD} to GND | -0.5V to 6.5V |
| Voltage on Any Pin (except DV) to GND ³ | -0.5V to $V_{DD}+0.5V$ |
| Voltage on DV to GND ⁴ | $\pm 15V$ |
| Power Dissipation | 50 mW |

Note 3: Voltages on pins other than DV, GND or V_{DD} may exceed 0.5 volt above or below the supply voltages provided the current is limited to 1 mA.

Note 4: The application of DV voltages higher than required to bring the output to positive full scale may cause device damage.

*** NOTICE:** Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at or above these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

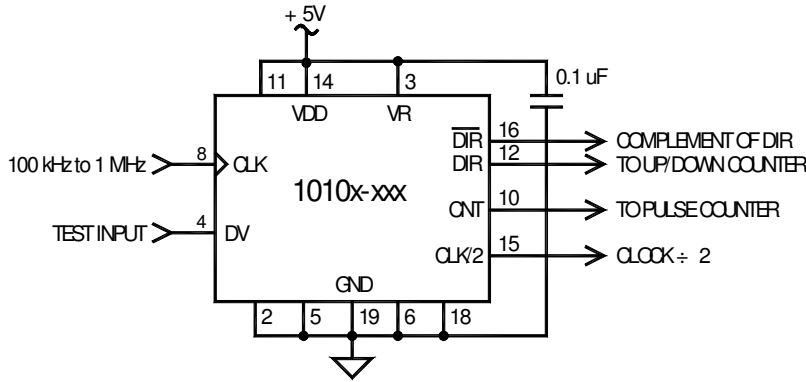
D.C. CHARACTERISTICS: $V_{DD}=V_R=5.0$ VDC, $T_C= 55$ to +125°C

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS | TEST CONDITIONS |
|-----------------|--|----------------|-----|-----|---------|---------------------------|
| V_{T-} | Negative Going Threshold Voltage (CLK) | 0.9 | 1.7 | | V | |
| V_{T+} | Positive Going Threshold Voltage (CLK) | | 3.0 | 3.7 | V | |
| V_H | Hysteresis Voltage (CLK) | 0.5 | 1.3 | | V | |
| V_{OL} | Output Low Voltage (CNT, DIR, CLK/2) | | | 0.4 | V | $I_{OL} = 2.0$ mA |
| V_{OH} | Output High Voltage (CNT, DIR, CLK/2) | $V_{DD} - 0.4$ | | | V | $I_{OH} = 2.0$ mA |
| I_I | Input Leakage Current (CLK) | | | 10 | μ A | $V_I = 0$ to V_{DD} |
| C_{IO} | Pin Capacitance | | | 10 | pF | 1 MHz, $T_A = 25^\circ$ C |
| $I_{DD}+I_{VR}$ | Operating Current | | 2 | 3 | mA | $F_{CLK} = 250$ kHz |

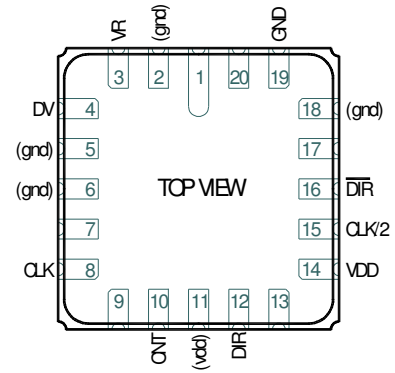
A.C. CHARACTERISTICS: $V_{DD}=V_R=5.0$ VDC, $T_C= -55$ to +125°C, Load Capacitance=50pF.

| PARAMETER | MIN | TYP | MAX | UNITS |
|-----------------------------|-----|-----|------|-------|
| CLK input frequency | 100 | 250 | 1000 | kHz |
| CLK input rise/fall time | | | 50 | ns |
| CLK duty cycle | 45 | 50 | 55 | % |
| CLK fall to DIR fall | 40 | 85 | 195 | ns |
| CLK fall to DIR rise | 40 | 90 | 205 | ns |
| CLK rise to valid CNT out | 40 | 90 | 230 | ns |
| CLK fall to CNT fall | 40 | 85 | 205 | ns |
| CLK fall to CLK/2 rise/fall | 40 | 90 | 210 | ns |

SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE



RECOMMENDED CONNECTIONS



PINOUT (LCC & JLCC)

USING THE COUNT (CNT) OUTPUT: Pulses from the CNT output are meant to be accumulated in a hardware counter. Each pulse accumulation or sample, reflects the average acceleration (change in velocity) over that interval. The sample period or “gate time” over which these pulses are accumulated determines both the bandwidth and quantization of the measurement.

$$\text{Quantization (g's)} = \frac{g_{SPAN} \cdot f_{SR}}{f_{CLK}}$$

$$f_{CNT} = f_{CLK} \left(\frac{1}{2} + \frac{g_{FORCE}}{g_{SPAN}} \right)$$

$$g_{FORCE} = g_{SPAN} \left(\frac{f_{CNT}}{f_{CLK}} - \frac{1}{2} \right)$$

Where:

$g_{SPAN} = 2*$ (full scale acceleration in g's)

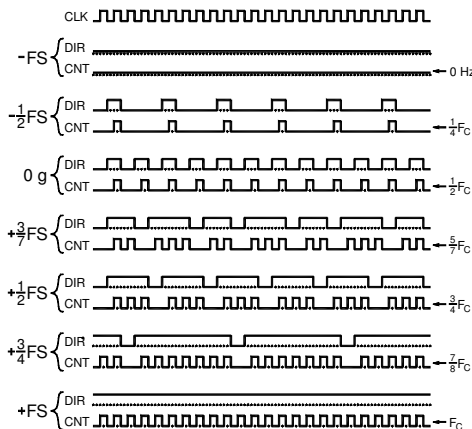
$f_{SR} =$ CNT sample rate in Hertz

$f_{CLK} =$ accelerometer clock rate in Hertz

$f_{CNT} =$ CNT pulse rate in pulses/sec

$g_{FORCE} =$ acceleration in gravity units

1 g = 9.8085 m/s² or 32.180 ft/s²



The first equation above shows that as the sample rate is reduced (i.e. a longer sample period), the quantization becomes finer but bandwidth is reduced. Conversely, as the sample rate is increased, quantization becomes coarser but the bandwidth of the measurement is increased. The second and third equations show how the CNT pulse frequency equates to the applied g-force. When using a frequency counter to monitor the CNT output pulse rate, a counter with a DC coupled input must be used. The CNT output is a return-to-zero signal whose duty cycle varies from zero to fifty percent, from minus full scale to positive full scale acceleration. A frequency counter with an AC coupled input will provide an erroneous reading as the duty cycle varies appreciably from fifty percent. The figure to the left illustrates how the CNT and DIR outputs vary as the accelerometer is subjected to accelerations from minus full scale (-FS) to plus full scale (+FS).

DEFLECTION VOLTAGE (DV) TEST INPUT: This test input applies an electrostatic force to the sense element, simulating a positive acceleration. It has a nominal input impedance of 32 kΩ and a nominal open circuit voltage of 1/3 V_{DD}. For best accuracy during normal operation, this input should be left unconnected or connected to a voltage source equal to 1/3 of the V_{DD} supply. The change in output pulse rate (Δf) is proportional to the square of the difference between the voltage applied to the DV input (V_{DV}) and 1/3 V_{DD}. Only positive shifts in the output pulse rate may be generated by applying voltage to the DV input. When voltage is applied to the DV input, it should be applied gradually. The application of DV voltages greater than required to bring the output to positive full scale may cause device damage. The proportionality constant (k) varies for each device and is not characterized.

$$\Delta f \approx k \left(V_{DV} - \frac{1}{3} V_{DD} \right)^2$$

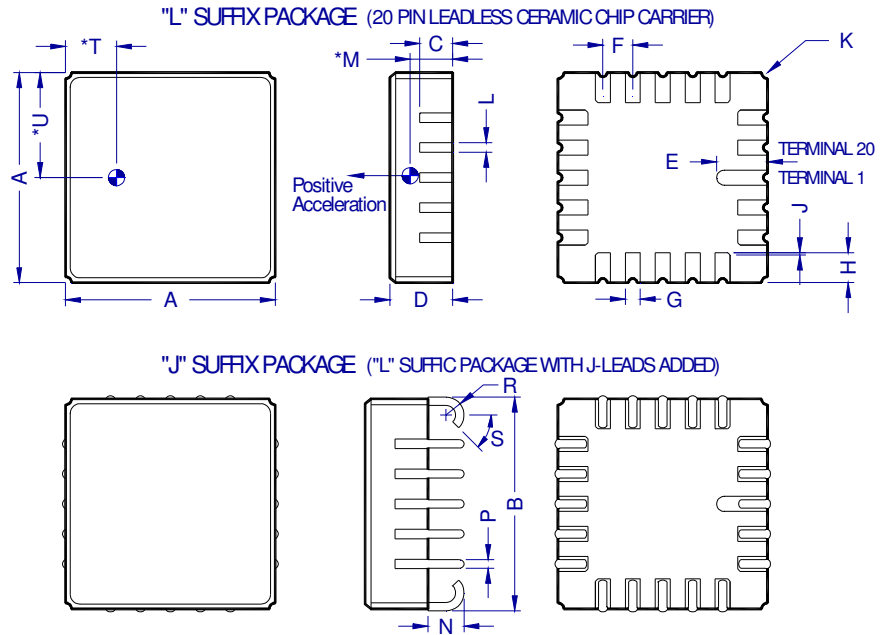
ESD and LATCH-UP CONSIDERATIONS: The model 1010 accelerometer is a CMOS device subject to damage from large electrostatic discharges. Diode protection is provided on the inputs and outputs but care should be exercised during handling to assure that the device is placed only on a grounded conductive surface. Individuals and tools should be grounded before coming in contact with the device. Do not insert the model 1010 into (or remove it from) a powered socket.



PACKAGE DIMENSIONS

- Notes:**
- * Dimensions 'm', 't' & 'u' locate acceleration sensing element's center of mass.
 - Lid is electrically tied to terminal 19 (GND).
 - Controlling dimension: inch.
 - Terminals are plated with 60 micro-inches min gold over 80 micro-inches min nickel. (This plating specification does not apply to the metallized pin-1 identifier mark on the bottom of the j-lead version of the package).
 - Package: 90% minimum alumina (black), lid: solder sealed kovar.

| Dim | Inches | | Millimeters | |
|-----|-------------|-------|-------------|------|
| | Min | Max | Min | Max |
| A | 0.342 | 0.358 | 8.69 | 9.09 |
| B | 0.346 | 0.378 | 8.79 | 9.60 |
| C | 0.055 TYP | | 1.40 TYP | |
| D | 0.095 | 0.115 | 2.41 | 2.92 |
| E | 0.085 TYP | | 2.16 TYP | |
| F | 0.050 BSC | | 1.27 BSC | |
| G | 0.025 TYP | | 0.64 TYP | |
| H | 0.050 TYP | | 1.27 TYP | |
| J | 0.004 x 45° | | 0.10 x 45° | |
| K | 0.010 R TYP | | 0.25 R TYP | |
| L | 0.016 TYP | | 0.41 TYP | |
| * M | 0.048 TYP | | 1.23 TYP | |
| N | 0.050 | 0.070 | 1.27 | 1.78 |
| P | 0.017 TYP | | 0.43 TYP | |
| R | 0.023 R TYP | | 0.58 R TYP | |
| * T | 0.085 TYP | | 2.16 TYP | |
| * U | 0.175 TYP | | 4.45 TYP | |



BIAS STABILITY CONSIDERATIONS

Bias temperature hysteresis can be minimized by temperature cycling your model 1010 accelerometer after it has been soldered to your circuit board. If possible, the assembled device should be exposed to ten cycles from -40 to +85°C minimum (-55 to +125°C recommended). The orientation to the Earth's gravitational field during temperature cycling should preferably be in the same orientation as it will be in the final application. The accelerometer does not need to have power applied during this temperature cycling.

SOLDERING RECOMMENDATIONS

RoHS Compliance: The model 1010 does not contain elemental lead and is RoHS compliant.

WARNING: If no-lead solder is to be used to attach the device, we do not recommend the use of reflow soldering methods such as vapor phase, solder wave or hot plate. These methods impart too much heat for too long of a period of time and may cause excessive bias shifts. For no-lead soldering, we only recommend the manual "Solder Iron Attach" method (listed on the next page of this data sheet). We also do not recommend the use of ultrasonic bath cleaners because these models contain internal gold wires that are thermo sonically bonded.

Reflow of Sn62 or Sn63 type solder using a hotplate is the preferred method for assembling the model 1010 surface mount accelerometer to your Printed circuit board. Hand soldering using a fine tipped soldering iron is possible but difficult without a steady hand and some form of visual magnification due to the small size of the connections. When using the hand solder iron method, it's best to purchase the J-Leaded version (1010J) for easier visual inspection of the finished solder joints.

Pre-Tinning of Accelerometer Leads is Recommended: To prevent gold migration embrittlement of the solder joints, it is best to pre-tin the accelerometer leads. We recommend tinning one lead at a time, to prevent excessive heating of the accelerometer, using a fine-tipped solder iron and solder wire. The solder bath method of pre-tinning is not recommended due to the high degree of heat the interior of the device gets subjected to which may cause permanent shifts in the bias and/or scale factor.

SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE



Hotplate Attach Method using Solder Paste or Solder Wire: Apply solder to the circuit board’s pads using Sn62 or Sn63 solder paste or pre-tin the pads using solder and a fine tipped soldering iron. If pre-tinning with an iron, apply flux to the tinned pads prior to placing the components. Place the accelerometer in its proper position onto the pasted or tinned pads then place the entire assembly onto a hotplate that has been pre-heated to 250°C. Leave on hotplate only long enough for the solder to flow on all pads (DO NOT OVERHEAT!)

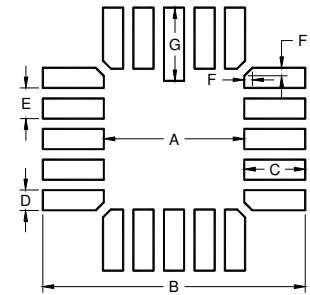
Solder Iron Attach Method using Solder Paste: Apply solder paste to the circuit board’s pads where the accelerometer will be attached. Place the accelerometer in its proper position onto the pasted pads. Press gently on the top of the accelerometer with an appropriate tool to keep it from moving and heat one of the corner pads, then an opposite corner pad with the soldering iron. Make sure the accelerometer is positioned so all 20 of its connections are centered on the board’s pads. Once the two opposite corner pads are soldered, the part is secure to the board and you can work your way around soldering the remaining 18 connections. Allow the accelerometer to cool in between soldering each pin to prevent overheating.

Solder Iron Attach Method using Solder Wire: Solder pre-tin two opposite corner pads on the circuit board where the accelerometer will be attached. Place the accelerometer in its proper position onto the board. Press gently on the top of the accelerometer and heat one of the corner pads that were tinned and the part will drop down through the solder and seat on the board. Do the same at the opposite corner pad that was tinned. Make sure the accelerometer is positioned so all 20 of its connections are centered on the board’s pads. Once the two opposite corner pads are soldered, the part is secure to the board and you can work your way around soldering the remaining 18 connections. Allow the accelerometer to cool in between soldering each pin to prevent overheating.

LCC & JLCC Solder Contact Plating Information: The plating composition and thickness for the solder pads and castellations on the “L” suffix (LCC) package are 60 to 225 micro-inches thick of gold (Au) over 80 to 350 micro-inches thick of nickel (Ni) over a minimum of 5 micro-inches thick of moly-manganese or tungsten refractory material. The leads for the “J” suffix (JLCC) package are made of an Iron-Nickel sealing alloy and have the same gold over nickel plating thicknesses as for the LCC pads.

Recommended Solder Pad Pattern: The recommended solder pad size and shape for both the LCC and J LCC packages is shown in the diagram and table below. These dimensions are recommendations only and may or may not be optimum for your particular soldering process.

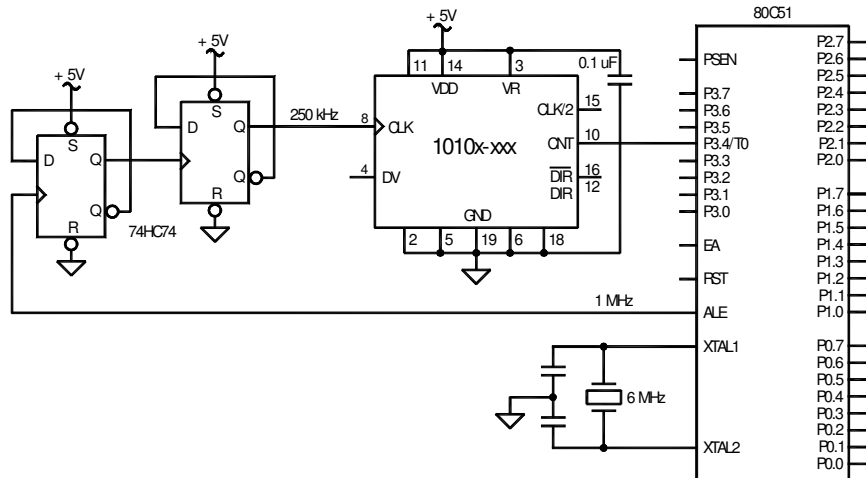
| DIM | Inch | mm |
|-----|------|-------|
| A | .230 | 5.84 |
| B | .430 | 10.92 |
| C | .100 | 2.54 |
| D | .033 | 0.84 |
| E | .050 | 1.27 |
| F | .013 | 0.33 |
| G | .120 | 3.05 |



APPLICATION NOTE: ACCELERATION MEASUREMENT WITH A MICROCONTROLLER

The CNT (count) pulse density modulation output of the model 1010 accelerometer was designed to drive the type of hardware pulse counter that is sometimes present in microcontrollers. The schematic (below) shows a model 1010 accelerometer driving the T0 counter of an Intel 80C51

microcontroller. The accelerometer clock is provided by the Address Latch Enable (ALE) output of the 80C51 after being divided by a factor of four by the two 74HC74 "D-Type" flip/flops. The divide by 4 is needed because the maximum count rate of the 80C51's T0 counter is 1/24th of the 8051's clock oscillator frequency (F_{OSC}) and the frequency of ALE is 1/6th of F_{OSC} . Divisors of greater than four should be used if F_{OSC} is greater than 12 MHz to keep the



SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE



accelerometer's clock frequency at or below the recommended 1 MHz maximum. Use of ALE for the accelerometer clock is only recommended for applications where no external memory is connected to the 80C51. ALE is missing an output pulse for each MOVX instruction, which is used to access external memory. Alternatively, any available clock source asynchronous with the 8051's clock may be used to drive the accelerometer so long as its frequency is between 100 kHz and 1 MHz and is no greater than 1/48th of F_{OSC}.

To obtain each interval's average acceleration, the software needs to poll counter T0's value at fixed intervals then subtract each new counter value from its previous value to obtain a delta (difference) count for each interval. Of course the software must also account for wraparound of the counter, which requires that the counter contain enough bits to prevent more than one counter overflow during each sample period. The delta count relates to the average applied acceleration according to the following equation.

$$\Delta C = \frac{f_{CLK} \left(\frac{1}{2} + \frac{A_g}{g_{SPAN}} \right)}{f_{SR}}$$

Where:

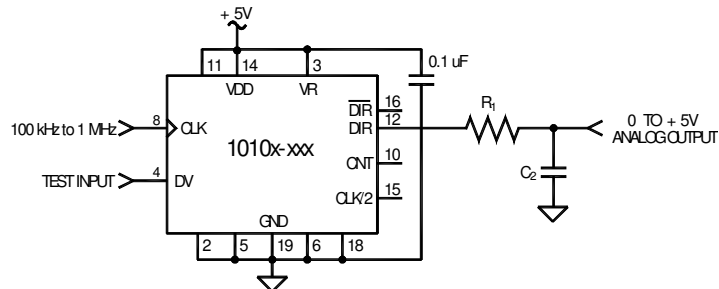
- ΔC = the change in the counter's value over each sample interval
- f_{CLK} = the accelerometer's input clock frequency
- A_g = the average acceleration force in g's during the sample interval
- g_{SPAN} = 2 * (full scale acceleration rating of accelerometer)
- f_{SR} = the software sample rate of the counter in samples/sec

At minus full-scale acceleration, the difference count (ΔC) is zero. Zero acceleration results in a difference count of one-half of the maximum difference count value; plus full scale acceleration results in the maximum value (f_{CLK}/f_{SR}). The actual difference value achieved at zero acceleration [which will be near $\frac{1}{2}(f_{CLK}/f_{SR})$], may be subtracted from each interval's difference count to obtain the acceleration count in sign-magnitude format.

CONVERTING DIR TO AN ANALOG VOLTAGE

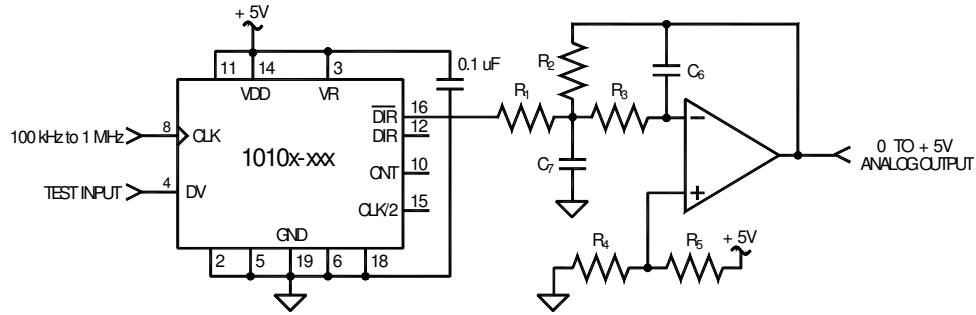
It is best to use a model 1210 or 1221 for analog applications but if a proportional analog voltage is desired from a model 1010, one can be easily generated by the connection of a low-pass filter to the DIR output as shown in the schematic (below). The table (at right) lists values for R1 and C2 for various cutoff frequencies (-3 dB frequency). R1 is chosen to be at least 100 times the maximum output impedance of DIR, which is 200Ω. The circuit or instrument that the 0 to +5V analog output is connected to, must have an input impedance at least 100 times the value of R1. This simple passive RC filter can be used as long as it provides sufficient rejection of the switching noise present on the DIR output for the specific application.

| CUTOFF FREQUENCY (Hz) | R1 (kΩ) | C2 (μF) |
|-----------------------|---------|---------|
| 200 | 36.0 | .022 |
| 800 | 35.7 | .0056 |
| 1000 | 34.0 | .0047 |
| 1600 | 30.1 | .0033 |
| 2000 | 36.0 | .0022 |



If greater rejection of switching noise is needed, a two pole active filter can be used as shown in the schematic (below). This circuit has the added advantage of providing very low output impedance compared with the single pole circuit. Its disadvantages include greater complexity and the need for 1 or 2 additional supply voltages for the op-amp. For both filter types, tight tolerance, temperature stable resistors and capacitors should be used. To reject common mode noise over long signal transmission line lengths, DIR and its complement can be used to drive a pair of wires with a differential filter placed at the far end of the wires.

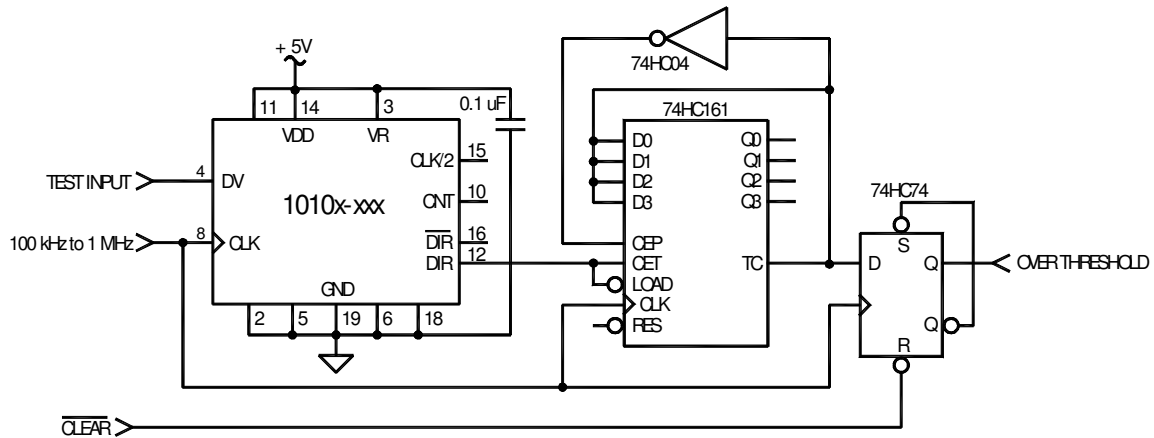
SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE



| Cutoff Frequency (Hz) | R1 & R2 (kΩ) | R3 (kΩ) | R4 & R5 (kΩ) | C6 (μF) | C7 (μF) |
|-----------------------|--------------|---------|--------------|---------|---------|
| 200 | 21.5 | 36.0 | 93.1 | .012 | .068 |
| 800 | 19.1 | 43.0 | 105 | .0027 | .018 |
| 1000 | 18.2 | 42.2 | 102 | .0022 | .015 |
| 1600 | 17.4 | 38.3 | 93.1 | .0015 | .010 |
| 2000 | 21.5 | 36.0 | 93.1 | .0012 | .0068 |

ACCELERATION THRESHOLD DETECTION:

For applications where it is desired to know when acceleration has exceeded a threshold value, the simple circuit shown in the schematic (below) can be used. This circuit uses a 74HC161 synchronous binary counter to detect when the DIR logic output goes high for a minimum of 16 clock cycles in a row. The 74HC74 D-type flip/flop is connected in a "ones-catch" configuration so that once the threshold is exceeded, the flip/flop stores the event. The clear input sets the counter value to zero and clears the flip/flop, making the circuit ready to detect the next 16 ones in a row sequence. When driven by the DIR (true) output, this circuit provides a threshold of approximately 3/4ths of full scale (+43.75g for a ±50g device). Negative acceleration pulses can be detected by connecting the counter to $\overline{\text{DIR}}$ instead of DIR.



SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE